

CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1. ~~(Currently Amended) A method of measuring signal skew on a programmable logic device, the device including a signal tree having a source node connected to first, second, and third destination branches, first, second, and third logic blocks programmably connectable to the respective first, second, and third destination branches, each of the logic blocks having an input terminal and an output terminal, the method comprising:~~
 - ~~a-~~ instantiating a first delay element on a programmable logic device, the device including a signal tree having a source node connected to first, second, and third destination branches, and first, second, and third logic blocks programmably connectable to the respective first, second, and third destination branches, each of the logic blocks having an input terminal and an output terminal, using a first programming sequence that includes:
 - ~~i-~~ connecting the first destination branch to the input terminal of the first logic block; and
 - ~~ii-~~ connecting the output terminal of the first logic block to the input terminal of the second logic block; and
 - ~~b-~~ instantiating a second delay element on the device using a second programming sequence that includes:
 - ~~i-~~ connecting the third destination branch to the input terminal of the third logic block; and
 - ~~ii-~~ connecting the output terminal of the third logic block to the input terminal of the second logic block; and

measuring signal skew on the programmable logic

device through the signal tree based on a difference in delay between the first and second delay elements.

2. (Original) The method of claim 1, wherein the signal tree is a clock tree.
3. (Original) The method of claim 1, wherein the input terminal of the second logic block is an asynchronous input terminal.
4. (Original) The method of claim 1, wherein the first, second, and third logic blocks are arranged on the device in a column.
5. (Previously Presented) The method of claim 4, wherein the second logic block is physically between the first and third logic blocks.
6. (Currently Amended) The method of claim 1, wherein the source node is further connected to fourth, fifth, and sixth destination branches and the programmable logic device further includes fourth, fifth, and sixth logic blocks programmably connectable to the respective fourth, fifth, and sixth destination branches, each of the logic blocks having an input terminal and an output terminal, the method further comprising:
 - ~~e-~~ instantiating a third delay element on the device using a third programming sequence that includes:
 - ~~i-~~ connecting the fourth destination branch to the input terminal of the fourth logic block; and
 - ~~ii-~~ connecting the output terminal of the fourth logic block to the input terminal of the fifth logic block; ~~and~~
 - ~~d-~~ instantiating a fourth delay element on the device using a fourth programming sequence that includes:
 - ~~i-~~ connecting the sixth destination branch to the

input terminal of the sixth logic block; and
~~ii.~~ connecting the output terminal of the sixth
logic block to the input terminal of the fifth
logic block; and
measuring signal skew on the programmable logic
device through the signal tree based on differences
in delay between at least two of the first, second,
third, and fourth delay elements.

7. (Currently Amended) A method of measuring signal skew on a programmable logic device, the device including a signal tree having a source node connected to first, second, and third destination branches, first, second, and third logic blocks programmably connectable to the respective first, second, and third destination branches, each of the logic blocks having an input terminal and an output terminal, wherein the source node is further connected to fourth, fifth, and sixth destination branches and the programmable logic device further includes fourth, fifth, and sixth logic blocks programmably connectable to the respective fourth, fifth, and sixth destination branches, each of the logic blocks having an input terminal and an output terminal, the method comprising:
- ~~a.~~ instantiating a first delay element on the device using a first programming sequence that includes:
 - ~~i.~~ connecting the first destination branch to the input terminal of the first logic block; and
 - ~~ii.~~ connecting the output terminal of the first logic block to the input terminal of the second logic block;
 - ~~b.~~ instantiating a second delay element on the device using a second programming sequence that includes:
 - ~~i.~~ connecting the third destination branch to the input terminal of the third logic block; and
 - ~~ii.~~ connecting the output terminal of the third logic block to the input terminal of the second

logic block

- e- instantiating a third delay element on the device using a third programming sequence that includes:
 - i- connecting the fourth destination branch to the input terminal of the fourth logic block; and
 - ii- connecting the output terminal of the fourth logic block to the input terminal of the fifth logic block; and
- d- instantiating a fourth delay element on the device using a fourth programming sequence that includes:
 - i- connecting the sixth destination branch to the input terminal of the sixth logic block; and
 - ii- connecting the output terminal of the sixth logic block to the input terminal of the fifth logic block,

wherein connecting the output terminal of the first logic block to the input terminal of the second logic block establishes a first net, connecting the output terminal of the second logic block to the input terminal of the second logic block establishes a second net, connecting the output terminal of the fourth logic block to the input terminal of the fifth logic block establishes a third net, and connecting the output terminal of the sixth logic block to the input terminal of the fifth logic block establishes a fourth net, the method further comprising defining the first and third nets to be identical and defining the second and fourth nets to be identical.

8. (Original) The method of claim 1, further comprising configuring the device to include the first and second delay elements in respective first and second oscillators.
9. (Original) The method of claim 8, further comprising comparing the periods of the first and second oscillators.

Claims 10-18 (canceled).

19. (Currently Amended) ~~A method of measuring clock skew on a programmable logic device, the programmable logic device including a clock distribution network having a source node connected to first, second, and third destination branches, and first, second, and third programmable logic blocks programmably connectable to the respective first, second, and third destination branches, each of the programmable logic blocks having an input terminal and an output terminal, the method comprising:~~

- a. programming a programmable logic device, the programmable logic device including a clock-distribution network having a source node connected to first, second, and third destination branches, and first, second, and third programmable logic blocks programmably connectable to the respective first, second, and third destination branches, each of the programmable logic blocks having an input terminal and an output terminal, to include a first ring oscillator in which the first destination branch is connected to the input terminal of the first logic block and the output terminal of the first logic block is connected to the input terminal of the second logic block; and
- b. after programming the programmable logic device to include the first ring oscillator, programming the programmable logic device to include a second ring oscillator in which the third destination branch is connected to the input terminal of the third logic block and the output terminal of the third logic block is connected to the input terminal of the second logic block; and
measuring clock skew on the programmable logic device through the clock-distribution network based on a difference between oscillation period of the first

ring oscillator and oscillation period of the second ring oscillator.

20. (Previously Presented) The method of claim 19, wherein the input terminal of the second logic block is an asynchronous input terminal.
21. (Previously Presented) The method of claim 19, wherein the first, second, and third logic blocks are arranged on the programmable logic device in a column.
22. (Previously Presented) The method of claim 21, wherein the second logic block is physically between the first and third logic blocks.
23. (Currently Amended) The method of claim 19, wherein the source node is further connected to fourth, fifth, and sixth destination branches and the programmable logic device further includes fourth, fifth, and sixth programmable logic blocks programmably connectable to the respective fourth, fifth, and sixth destination branches, each of the programmable logic blocks having an input terminal and an output terminal, the method further comprising:
- ~~e-~~ programming the programmable logic device to include a third ring oscillator in which the fourth destination branch is connected to the input terminal of the fourth logic block and the output terminal of the fourth logic block is connected to the input terminal of the fifth logic block; ~~and~~
 - ~~d-~~ programming the programmable logic device to include a fourth ring oscillator in which the sixth destination branch is connected to the input terminal of the sixth logic block and the output terminal of the sixth logic block to the input terminal of the

fifth logic block; and
measuring clock skew on the programmable logic device
through the clock-distribution network based on
differences in oscillation period between at least
two of the first, second, third, and fourth ring
oscillators.

24. (Previously Presented) The method of claim 23, wherein connecting the output terminal of the first logic block to the input terminal of the second logic block establishes a first net, connecting the output terminal of the second logic block to the input terminal of the second logic block establishes a second net, connecting the output terminal of the fourth logic block to the input terminal of the fifth logic block establishes a third net, and connecting the output terminal of the sixth logic block to the input terminal of the fifth logic block establishes a fourth net, the method further comprising defining the first and third nets to be identical and defining the second and fourth nets to be identical.
25. (Previously Presented) The method of claim 19, further comprising configuring the programmable logic device to include the first and second delay elements in respective first and second oscillators.
26. (Previously Presented) The method of claim 25, further comprising comparing the periods of the first and second oscillators.